Active Pixel Sensor (APS) Testbed

Michael P. Brenner
Carl Christian Liebe
Robert C. Stirbl
Larry Avril
Bedabrata Pain

Abstract

A new photon sensitive imaging array – Active Pixel Sensor (APS) – has emerged as a potential replacement to conventional Charged-Coupled Device's (CCD). The APS chips utilize existing Complementary Metal Oxide Semiconductor (CMOS) production facilities, and the technology has several advantages over CCD technology. These include lower power consumption, higher dynamic range, higher blooming threshold, individual pixel readout, single 3.3 or 5 volt operation, the ability to integrate on-chip timing, control, windowing, Analog to Digital (A/D) conversion, centroiding operations and low cost.

The latest generation of APS has evolved to a fully digital camera on a chip. The JPL designed APS Digital Integrated Camera Experiment (DICE) has a five wire interface. The five wire interface include the power, ground, clock, serial data in and serial data out. The serial data in allows for control of continuous or still imaging and full programmability of resolution, speed, electronic pan and zoom, exposure and data reduction. The APS DICE requires a single bias voltage and has on chip bias generation and a 10-bit A/D converter. The power consumption is less than 20mW, and the maximum data rate is 50Mbits/second.

The testbed developed for APS characterization consists of three subsystems. The first subsystem is the sensor board. The sensor board contains DICE APS sensor and the drive electronics for the interface signals. This unit is placed in a vacuum chamber, so it can be cooled without condensation. The APS Interface Electronics is the second subsystem. The APS interface electronics contains the Complex Programmable Logic Device (CPLD), test support electronics, 422 drivers that interface with the frame grabber and the UART interface that communicates with the PC. The PC is the third subsystem and performs two functions. One function is to host the Imaging Technology™ Frame Grabber that receives the data from the sensor formatted by the CPLD. The second function is to provide a windows based interface to command the APS sensor.

The system has been used to characterize prototypes of the DICE chip. This characterization included measurement of full well, dark current, effective number of bits in the converter, pixel to pixel variation, conversion factor and quantum efficiency. The results of this characterization will be presented in this paper.

Currently, the DICE is a candidate for two specific applications at JPL. One application is to use the APS DICE as a potential replacement for CCD star trackers. Star trackers provide attitude estimation onboard most 3 axis stabilized spacecraft. The spacecraft attitude is calculated based on observed positions of stars, which are located and identified in an image of the sky. Another application is a military project called Viewing Imager Gimballed Instrumentation Laboratory Analog Neural Three-dimensional Processing Experiment (VIGILANTE). The VIGILANTE project is a planned vision system capable of tracking and recognizing targets real time, on a small airborne platform. The DICE will be used as the visible sensor operating at real time rates.